

### **REMARKS**

Claims 47-58 are pending. Previously pending claims 35-44 were canceled. New claims 47-56 correspond with respective claims 35-44 and address the outstanding rejections under 35 U.S.C. § 101, § 102/103 and § 112.

No new matter was added. The first blocker, the intra-permuter, the second blocker and inter-permuter and described throughout the specification. The limitation wherein the first blocker, the intra-permuter, the second blocker and inter-permuter are operated overlapped in time is disclosed in at least paragraph [046] spanning pages 19-20 of the present specification, and the corresponding Figs. 2A-2C and Figs. 5A-5B associated with this text. New dependent claims 57 and 58 are likewise disclosed by at least these specification excerpts and figures.

For at least the reasons set forth below, withdrawal of all outstanding rejections as they relate to new claims 47-58 is respectfully requested.

### ***Drawings***

Replacement sheets for Fig. 4 and Figs. 5A and 5B are attached hereto. These replacements sheets supersede all previously submitted formal drawings for these figures.

### ***35 U.S.C. § 112, first and second paragraph, rejections***

None of the new claims 47-58 refer to “turbo codes.” Accordingly, these rejections are now believed to be moot as they relate to the new claims.

### ***35 U.S.C. § 101 rejection***

All of the new claims explicitly recite the physical elements that perform the algorithmic functions and thus are believed to be clearly directed to statutory subject matter. The new claims thus do not recite merely recite abstract algorithms. Accordingly, withdrawal of this rejection is respectfully requested as it relates to the new claims.

***Prior Art Rejections***

Claims 35-37 and 39-41 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by the 3GPP document. Claims 38 and 43-44 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the 3GPP document in view of Kim. Claim 42 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over the 3GPP document in view of Suda. Withdrawal of these rejections as they pertain to the new claims is respectfully requested.

1. Patentability of independent claims 47, 50, 51 and 55 over the 3GPP document

Each of the new claims recites that “the first blocker, the intra-permutter, the second blocker and inter-permutter are operated overlapped in time” which is an inherent feature of the presently claimed algorithm. In contrast, the algorithm described in the 3GPP document does not operate these elements overlapped in time. Instead, certain elements are operated sequentially. For example, intra-block permutations must be completed before inter-block permutations can be started. By performing intra-block permutations and inter-block permutations overlapped in time, the present invention can complete the interleaving process quicker than the sequential process described in the 3GPP document. That is, overall interleaving latency is reduced compared to the 3GPP process.

The following time diagram example illustrates how intra-block permutations and inter-block permutations are performed overlapped in time in the present invention, in contrast to the non-overlapping manner described in the 3GPP document:

Consider that there are  $M=5$  blocks and that  $D=1$ .  $IA(i)$  is the intra-block permutation of the  $i$ -th block, and  $IR(i)$  is the inter-block permutation of the  $i$ -th block.

T=1	T=2	T=3	T=4	T=5	T=6	T=7
IA (1)	IA(2)	IA(3)	IA(4)	IA(5)		
		IR(1)	IR(2)	IR(3)	IR(4)	IR(5)

Table 1: An exemplary time diagram of the interleaver in the present invention

T=1	T=2	T=3	T=4	T=5	T=6	T=7	T=8	T=9	T=10
IA (1)	IA(2)	IA(3)	IA(4)	IA(5)					
					IR(1)	IR(2)	IR(3)	IR(4)	IR(5)

Table 2: An exemplary time diagram of the 3GPP documented interleaver

As illustrated above, in the present invention, the inter-block permutation can be performed after the first and the second blocks are permuted. In contrast, inter-block permutation cannot be performed in the scheme described in the 3GPP document until inter-block permutation is completed for all five blocks.

Referring to Applicants's specification, one preferred embodiment of the present invention that shows the overlapping feature is described, in part, in paragraph [046] spanning pages 19-20, repeated herein for convenience (underlining added for emphasis):

FIG. 5A and 5B illustrate timing diagrams 500 for operations of the exemplary primary encoder 105, secondary encoder 106, and interleaver 107. As previously described, the interleaver 107 groups the source sequence of symbols X 101 into the sequence of blocks 205. With reference also to FIGS. 2A-2C, a timing line 501 is segmented into equal units of data, wherein a block of length L 209 symbols in the source sequence X 101 is one unit. The blocks in the timing line 501 are labeled block 0, block 1, block 2, and so forth. For example, intra-block permutation begins immediately at a start of block 0 502 once the source sequence of symbols X 101 is available. After one full block of the sequence of blocks 205 is intra-permuted by the intra-permuter 202, the second blocker 203 begins at a start of block 1 503 to group the sequence of intra-permuted symbols 206 into the sequence of intra-permuted blocks 207. The inter-permuter 204 begins at the start of block 1 503 to interleave the sequence of intra-permuted blocks 207 across the number of blocks B 210. The interleaver 107 begins outputting at a start of block B+1 504 the sequence of interleaved symbols 108 after B blocks 210 have been inter-permuted. For example, if the number of blocks B 210 is three, then B+1 is equal to four. The primary encoder 105 begins encoding immediately at the start of block 0 502 once the source sequence of symbols X 101 is available. The secondary encoder 106 begins encoding at the start of block B+1 504 once the sequence of interleaved symbols 108 becomes available.

Nor do Kim or Suda make up for the above-noted deficiencies in the 3GPP document. In the outstanding Office Action, the Examiner asserts that Fig. 5 of Suda teaches simultaneous inter-block and intra-block permutations. This is incorrect. Fig. 5 of Suda is described on column 5, line 14 through column 8, line 4. Fig. 5 is also depicted in Fig. 10. Referring to this text portion, the second stage 42 performs intra-permutation and corresponds to steps 105-108 shown in Fig. 10. The third stage 43 performs inter-permutation and corresponds to step 109 shown in Fig. 10. Step 109 occurs after steps 105-108, not simultaneously with steps 105-108. In sum, Suda teaches away from simultaneous intra-block and inter-block permutations.

### 3. Patentability of dependent claims

The dependent claims are believed to be patentable over the applied references for at least the reason that they are dependent upon allowable base claims and because they recite additional patentable elements and steps.

### *Conclusion*

Insofar as the Examiner's rejections were fully addressed, the instant application is in condition for allowance. Issuance of a Notice of Allowability of all pending claims is therefore earnestly solicited.

Respectfully submitted,

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Enclosure (2 replacement sheets)